

WHAT IS CLAIMED IS:

1           1.       A multi-chip module (MCM) comprising:  
2           a first integrated circuit (IC) chip on a substrate;  
3           a first ground plane coupled to the first IC chip;  
4           a second IC chip on the substrate; and  
5           a second ground plane coupled to the second IC chip.

1           2.       The MCM of Claim 1, wherein each of the first and second ground  
2           planes is coupled to at least one external lead of the MCM.

1           3.       The MCM of Claim 1, wherein each of the first and second ground  
2           planes is formed as a respective trace on the substrate.

1           4.       The MCM of Claim 1, wherein each of the first and second ground  
2           planes is substantially rigid.

1           5.       The MCM of Claim 1, wherein each of the first and second ground  
2           planes is substantially flexible.

1           6.       The MCM of Claim 1, wherein each of the first and second ground  
2           planes comprises a strip of conductive material.

1           7.       The MCM of Claim 1, wherein each of the first and second ground  
2           planes comprises a layer of conductive material.

1           8.       The MCM of Claim 1, wherein each of the first and second ground  
2           planes comprises a substantially solid layer of conductive material.

1           9.       The MCM of Claim 1, wherein each of the first and second ground  
2 planes comprises a grid of conductive material.

1           10.     The MCM of Claim 1, wherein the first chip is bonded to the first ground  
2 plane, and the second chip is bonded to the second ground plane.

1           11.     The MCM of Claim 1, wherein the first chip is attached to the first  
2 ground plane, and the second chip is attached to the second ground plane.

1           12.     The MCM of Claim 1, wherein at least one of the first and second chip  
2 comprises a dynamic random access memory (DRAM) chip.

1           13.     The MCM of Claim 12, wherein the first and second chips are attached  
2 to the first and second ground planes via a flip-chip technique.

1           14.     The MCM of Claim 1, wherein at least one of the first and second chips  
2 comprises a memory chip.

1           15.     The MCM of Claim 1, wherein at least one of the first and second chip  
2 comprises an application specific integrated circuit (ASIC).

1           16.     The MCM of Claim 1, wherein one of the first and second chips is  
2 coupled to a plurality of input/output connectors of the MCM and the other of the first  
3 and second chips is not coupled to any input/output connectors of the MCM.

1           17.     The MCM of Claim 1, wherein the first chip is coupled to the second  
2 chip via at least one trace.

1            18.     The MCM of Claim 1, wherein at least one of the first and second chips  
2 may be tested without affecting operation of the other of the first and second chips in  
3 the MCM.

1            19.     The MCM of Claim 1, wherein at least one of the first and second chips  
2 may be tested without being affected by an operation of one or more other chips in the  
3 MCM.

1            20.     The MCM of Claim 1, further comprising:  
2 a first power plane coupled to the first IC chip; and  
3 a second power plane couple to the second IC chip.

1            21.     A method of testing first and second integrated circuit (IC) chips on a  
2 substrate in a multi-chip module, the first IC chip provided with a first ground  
3 plane and the second IC chip provided with a second ground plane, the method  
4 comprising:  
5 testing the first IC chip without affecting an operation of the second IC chip; and  
6 testing the second IC chip without affecting an operation of the first IC chip.

1            22.     A method of testing first and second integrated circuit (IC) chips on a  
2 substrate in a multi-chip module, the first IC chip provided with a first ground plane and  
3 the second IC chip provided with a second ground plane, the method comprising:  
4 testing the first IC chip without being affected by an operation of the second IC  
5 chip; and  
6 testing the second IC chip without being affected by an operation of the first IC  
7 chip.

1            23.     A method of testing at least one interconnect between two integrated  
2 circuit (IC) chips on a substrate in a multi-chip module, the first IC chip provided with a  
3 first ground plane and the second IC chip provided with a second ground plane, the  
4 method comprising:

1           applying a signal to the first IC chip; and  
2           determining a current change on the interconnect in response to the signal  
3           applied to the first IC chip.

1           24.     A method of making a multi-chip module (MCM) comprising:  
2           providing a substrate;  
3           providing a first ground plane and a second ground plane on the substrate; and  
4           providing a first integrated circuit (IC) chip for the first ground plane and a  
5           second IC chip for the second ground plane.

1           25.     The method of Claim 24 comprising providing a first power plane for the  
2           first chip and a second power plane for the second chip.

1           26.     The method of Claim 24 comprising attaching the first and second  
2           ground planes to the substrate.

1           27.     The method of Claim 26, wherein testing the first IC chip comprises  
2           supplying power to the first IC chip without supplying power to the second IC chip.

1           28.     The method of Claim 26 comprising attaching the first and second chips  
2           to the substrate.

1           29.     The method of Claim 24, wherein testing the first IC chip comprises  
2           supplying power to the first IC chip without supplying power to the second IC chip.

1           30.     The MCM of Claim 29, wherein the first power plane supports a first  
2           voltage level and the second power plane supports a second power level.

1           31.     The MCM of Claim 29, further comprising a third power plane coupled  
2     to both first and second IC chips.